

Acoustic Pinger Locator (APL) Subsystem

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Abstract — The overall goal of this project is to create a subsystem, the Acoustic Pinger Locator (APL), and have it recognize an underwater acoustic waveform being produced by a pinger at a specific frequency and then localize a relative position from the APL subsystem to the pinger. After this prototype is designed, constructed, and tested, it will be utilized on the Autonomous Underwater Vehicle (AUV) of the Robotics Club at UCF to compete in the Association for Unmanned Vehicle Systems International (AUVSI) and the Office of Naval Research's (ONR) 13th International AUV Competition in San Diego, California. The APL system will utilize both analog and digital hardware for accomplishing the task. The analog hardware is used for conditioning the signal through amplification and filtering for the specified pinger frequency. The digital hardware will control most of the analog hardware and perform the acoustic localization mathematical techniques on the acquired data.

Index Terms — Acoustic localization, multilateration, FPGA, hydrophones, band-pass filter, variable gain amplifier.

I. INTRODUCTION

The preliminary design consists of an array of four to five hydrophones arranged in a particular way to allow for phase analysis on the signals to triangulate a heading, depth, and distance to the underwater acoustic pinger. Several different techniques were researched to achieve acoustic localization; a simulator was created to perform some preliminary analysis on these different methods to facilitate a final design. Another important aspect of this project is to receive the acoustic pinger signals from the underwater environment. The proposed method of achieving this goal is a passive hydrophone array mounted on the vehicle that converts acoustic energy into electrical energy. These attenuated signals are then conditioned by first pre-amplification with a variable gain to a utilizable signal. The signal is then filtered at the pinger's specified

frequency using a fourth order Butterworth bandpass filter to remove unwanted noise. The final analog signal processing stage needs to adjust the signal for the appropriate range of the analog to digital converter.

The analog signals are captured simultaneously from the analog to digital converter at a sampling rate that exceeds the Nyquist sampling theorem to receive unaliased digital signal data. The data is then processed by a field programmable gate array (FPGA) which contains the digital signal processing to calculate the acoustic localization of the pinger. The first step is to analyze each individual hydrophone signal by performing the Fast Fourier Transform (FFT) on the signals and determine relative phase differences between the hydrophone signals. The phase differential information is then used in the mathematical multilateration technique implemented on the FPGA to calculate the pingers location. The pingers heading, depth, and distance relative to the hydrophone array is then communicated over serial to the AUV's host computer which is then used to navigate to the pinger in the competition.

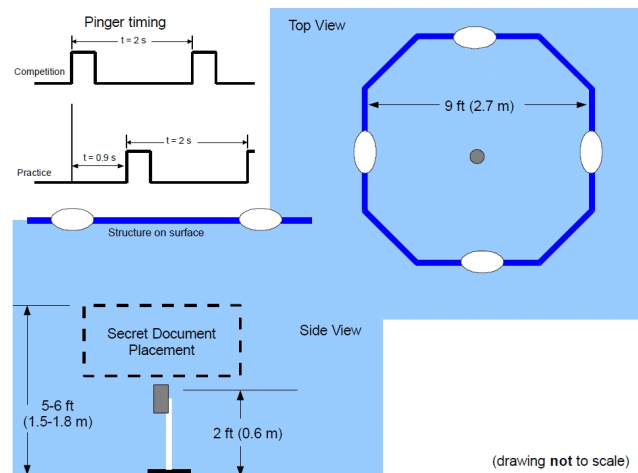


Fig. 1. The signal produced by the pinger along with several physical dimensions associated with the pinger mission.

II. DIGITAL HARDWARE

A. Digilent Nexys2 FPGA Development Board

The hardware selection is one of the most important parts of this project. There are quite a lot of different implementations and combinations of boards we can use to complete our design. We have come to the conclusion of using FPGA for our design. One of advantages of using FPGA is it can be used to program to do whatever users need; it is very scalable and flexible with user's needs and can be dynamically changed.

Nexys2 FPGA Board is one of our top choices of the FPGA board; it is a very powerful digital system design device. It has Xilinx Spartan 3E FPGA build in the device itself. It includes a 16 Mbytes of the fast SDRAM along with 16 Mbytes of Flash ROM, this board has the Xilinx's 32-bit RISC Microblaze™ embedded on-board. This board can accomplish most of the designs without any complications, thanks to the building high-speed USB2 with fast transfer rate. It has plenty of the I/O devices, expansion ports, and many of the data ports allows for more freedom of input and output the data and device connections. The cost of the board is inexpensive; it cost \$149 with Academic discount for 1200 gate version. To utilize and communicate with the board, we need to use the free program from Digilent called Digilent Adept Suite and Xilinx ISE WebPack Design Software.

USB cable will be use to power the board and to provide the data transfer. We have to set the power jumper to USB side in order for the board to get the power. The USB cable to the board (small USB side) and connect the other side of USB (the regular at side) to the computer. After the setting is done, we can switch on the power anytime by switching the device on in the North West corner of the board. The power LED will then turn on to indicate the board itself has power.

The board has a build in self-test, so we can do a self-test to make sure all the functions are working. To do this, we need to set the jumper JP9 in the middle of the North East corner of the board to ROM side, but to leave the JTAG side open. After the setting is done, we can switch on the power and press the reset button (Figure) at the North East corner to let it run. The seven segment display (Figure) should show a 4 Digit character and will display run for a short period of time, and then it should display PASS or 128 alternatively. Unless if there is something wrong with board itself, the PASS character should display on the screen. Alternately, we could perform the self test using the build in software Adept and click on Test tab.

B. PmodAD1

This signal capture process has to be done in the analog sense. It will then be process in the digital world. There are so many different approaches to do this. One way to accomplish this is to capture the signals in analog way, and the other way is capture the signal using A/D (Analog to Digital converter) to convert the analog signal and convert it to digital. There are thousands of types and makes of Analog to Digital converters in the market; they all have different specifications for each individual ones. Most of them have a lot of different sampling rates. Some questions we may ask ourselves are how fast can they sample? What type of techniques does it involve? How are

the actual sampling works? Base on our initial research, we thought that the Analog to Digital converter part that is provided by a company called Digilent would help us with this project. They actually make P mod module that will be use as Analog to Digital converter to process the signals. The price is really good for the performance and part that is involved. Also, this product shall provide us with high enough frequency.

One of the A/D converters we can use is the Pmod AD1. PmodAD1 is an Analog to Digital Module Converter board that can be use to connect to the Nexys2 FPGA board. Figure 5.3 below shows the device PmodAD1 and its pin connectors, which has two 12-bit A/D inputs and this device can help us converts the signals at a maximum capability of rate of one million samples per second, this will be sufficient enough for our device requirement. This device has 6 pins-header connectors, and the device is really compact which is smaller than 1 square inch, it come with a 6" 6-pin cable and a 6 pin header and it is ideal for any applications and can be located at any signal source. We can utilize this device to convert analog input signal from 0-3.3 volts to a 12 bit digital signal of 0 to 4095.

C. RS232

Developing a robust and simple communication system will provide a superior system for use in the Acoustic Pinger Locator Subsystem. Using a standard protocol that has already been developed and is supported by the current Autonomous Underwater Vehicle (AUV) of the UCF Robotics Club is an important feature for the APL Subsystem. Limiting the amount of conductors that have to be passed from the AUV System to the APL Subsystem while providing waterproof connections is important to minimize for both cost and eliminate system failures. Support for the protocol on a software and hardware end is another necessary feature for the APL Subsystem. Due to these constraints and features of the APL Subsystem the best choice by both us the Senior Design Team and recommendations from the Robotics Club, we have chose Asynchronous RS-232 Serial Communication Protocol, utilizing a standard baud rate over Data Transmit, Data Receive, and a common reference ground. For interfacing to the computer, the CxUtils library will be used.

Many systems support a simple asynchronous serial communication based on the RS-232 standard. The digital processor that is picked for the design will support RS-232. For the computer side a USB-to-Serial Adapter will be utilized for the serial support. A state machine will be used to control the hardware universal serial asynchronous receiver transmitter (USART) module for maintain proper communication to the on-board computer. With the on-

board computer the interface to the serial communication will be implemented with the cross platform utilities commonly used in the Robotics Club at UCF known as CxUtils which is hosted on the open source repository, Zebulon at sourceforget.net.

III. ANALOG HARDWARE

The analog hardware board is a necessary and important component of the overall system because it will act as the system's conditioning and noise removal step. It must complete this task without adding any distortion or noise to the amplitude and phase of the signal. Other features are that it is a very robust system, in that it is almost completely configurable through the FPGA/computer and does not have to be hand-tuned or physically adjusted by the users. This will be completed in three stages analog stages. The first being a pre-amplification stage that only amplifies the original signal. The second step then filters and amplifies the signal. The final stage then amplifies or attenuates the signal, based on the output of the second stage, and then conditions the signal for use by the ADCs (Analog to Digital Converters). This final signal can be seen in Figure 2. Additionally, the board will need to generate the necessary power from the raw 22.2 V batteries supplied by the AUV team. Another task of this board is to allow these analog components to communicate with the FPGA, which operates at different voltage levels than the analog components. The analog components discussed below describe a single channel. In the final circuit there will be five identical circuits on the board to accommodate up to five hydrophones, each having their own individual signal.

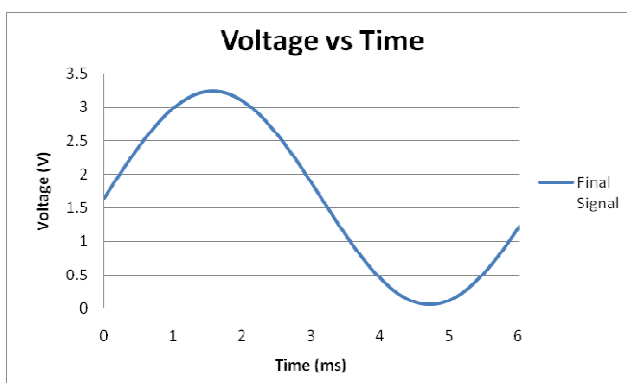


Fig. 2. This graph shows what the final waveform will look like once it has been amplified and filtered by the board. If a similar graph was produced with the raw signal, it would look like ground. Notice the signal is also shifted up to range from 0 to 3.3V for the ADCs.

A. Pre-Amplification Stage

The pre-amplification stage is the phase of the board that takes in the raw signal from the hydrophone and amplifies it. This will be a weak signal, generally averaging less than 10mV. This raw signal is taken into the board and immediately sent to an analog voltage controlled VGA (Variable Gain Amplifier). The specific chip being used is Analog Devices AD605. This chip contains two independently controlled VGAs that provide up to a 100dB gain each. The analog voltage that controls the VGA is controlled by a digital potentiometer, specifically the DS1803 by Maxim-IC. This chip also provides two independently controlled potentiometers. The potentiometers are adjusted by the FPGA over an I2C line. It has three address pins that allows for the use of up to eight chips, which results in the ability to use sixteen individually controlled digital potentiometers. The output of this stage is then sent to be filtered by the system.

B. Filtering Stage

The second stage then filters the incoming signal to remove noise while not adding any phase or signal distortion. Because a key feature of the APL system is to be adjustable, a programmable filter was used at this stage. The rules of the competition state that the pinger frequency can change between rounds, by using a filter that can be programmed through the FPGA interface the team will be able to quickly change the pinger they are trying to find. The MAX268 by Maxim-IC was chosen. This filter has two 2nd order bandpass filters per chip. It has a programmable center frequency, Q and has an additional gain stage. The filters will be used in series resulting in a 4th order bandpass filter, this is completed by sending the output of the first filter to the input of the second. The chip is programmed by setting the F and Q pins to +/- 5V and a variable frequency clock line that oscillates between +/- 5V. These are the equations provided in the datasheet for setting the center frequency, input clock frequency and Q:

$$f_{CLK}/f_0 = \pi(N+13) \quad (1)$$

$$Q = 64/(128-N) \quad (2)$$

Equation (1) is used to find the f_{clk} (clock frequency) when setting the f_0 (center frequency). It should be noted that a higher f_{CLK}/f_0 ratio results in a more continuous filtering of the signal. N in (1) is set by connecting pins $F_0 - F_4$ to logical high or low. Equation (2) on the other hand is used to set the Q, which for a bandpass filter, adjusts the

allowable frequencies around f_0 . N in (2) is set by connecting pins $Q_0 - Q_6$ to logical high or low.

The output of this stage provides environmental noise removal including echo and any other noise that might exist in the arena. This signal is then sent to the final stage.

C. Post-Amplification/Attenuation and Signal Conditioning

This final stage serves three purposes. The first is to amplify or attenuate the signal as necessary. Next the signal is adjusted to a voltage from -1.5 to 1.5V. The last step shifts the signal to 0 to 3.3V so that the ADCs can use the signal without being damaged.

The amplification/attenuation is done by feeding the signal into the second VGA on the AD605 chip used in the pre-amplification stage. A difference is that a relay may be activated that allows that VGA to attenuate the signal or deactivated to add another gain stage. This relay will be controlled with jumpers and have to be set at an earlier time. After this the signal is fed to an op-amp, specifically the MC33272 from ON Semiconductor. This is used in a non-inverting adder configuration. The signal it is being added with is a voltage from the DS1803 that is controlled by the FPGA, it will generally be about 1.65V. This circuit shifts the signal into the positive range from 0 to 3.3V. The op-amp is specifically powered off of 0 to 3.3V. This means that even if the signal goes out of bounds, it will hit the rails of the op-amp before reaching the ADCs. This provides protection from a signal that is amplified too much. In Figure 3 a schematic of a single channel can be seen.

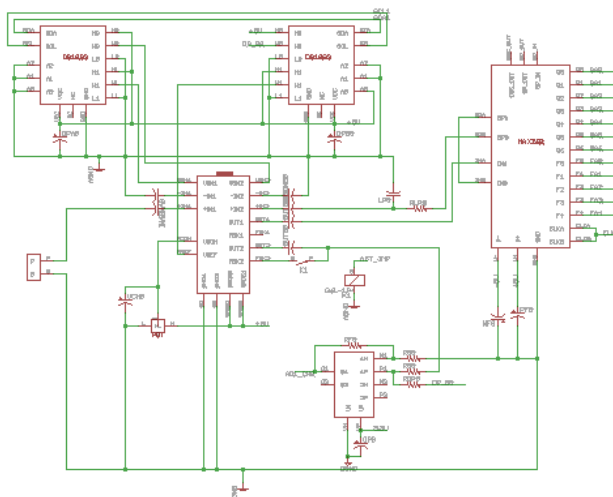


Fig. 3. This schematic shows the components used for a single channel. This will be multiplied four more times, to accommodate up to five hydrophones. The major devices shown include the AD605, DS1803, MAX268 and MC33272.

D. Power

The power to the board will be coming from the raw battery voltage. The AUV team is using 22.2V lithium polymer batteries, this mean the voltage may range from 20 to 24V. Another consideration is that several of these devices will need +/- 5V to properly run. To meet these requirements the JCJ0824D05 from XP Power was purchased. This device is 82% efficient and can take an input voltage from 18 to 36V. Each channel of the board draws about 60mA. When multiplied by the number of channels the current draw will be about 250mA. The device can handle this by being able to provide +/- 800mA, meets all the requirements.

The op-amps and ADCs will be running off of 3.3V which is provided by the FPGA.

E. Interfacing DS1083

As mentioned before the digital potentiometers are set by sending them a message over I2C. A problem that arises is that the voltage levels of the FPGA range from 0 to 3.3V while the digital potentiometer chip is expecting a voltage range of 0 to 5V. Because of this a buffer chip was used to solve the problem. The chip that was selected is the NXP P82896, which is specifically made to adjust I2C signal lines. It is able to adjust the SDA and SCL lines from 3.3 to 5V and not interfere with the messages being sent.

F. Interfacing the MAX268

The communication between the FPGA and filter are also a problem because the filter expects a logical low to be -5V and a logical high to be 5V for the F, Q and clock signal. This is impossible for the FPGA to provide so a MAX909 comparator chip from Maxim-IC was used. It is fast, so that it does not distort the clock signal, and only requires a reference voltage that will be set by a hand-adjusted potentiometer.

G. Board Layout

The board layout of the APL system is of particular importance because of how attenuated the original signal is and the necessity to remove any noise or distortion. This is further increased because the signal can also be at a relatively high frequency. Another issue is that because of size limitations the board must be relatively small. Because of the amount of traces, Eagle's auto-route feature was used to route the board. For the same reason a four layer board design was chosen. Figure 4 shows that most of the traces exist on the top and bottom layer. The second

layer acts as both the digital and analog ground, only connecting at the ADC junction. The third layer is 5V which is used by almost every component. Particular care was taken to have short traces at the initial input of the signal.

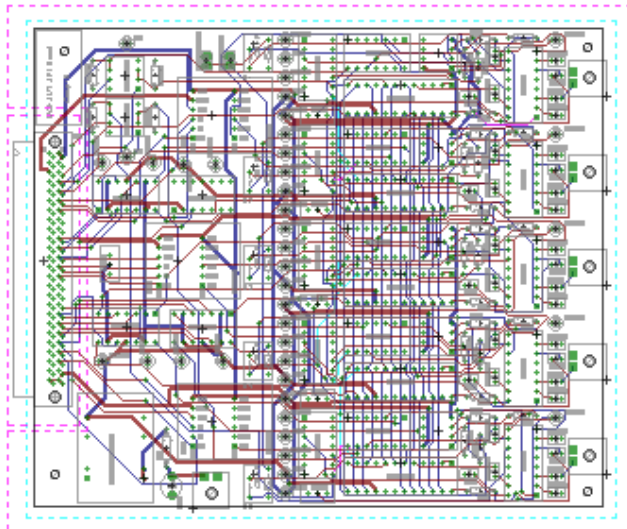


Fig. 4. This is the final board layout. It can support up to five hydrophones. Other components include the ADCs and components necessary to interface the FPGA exist on this board. The final dimensions are 6in x 5in.

The FPGA will connect directly to the analog board through the Hirose FX2 socket connector. Every connection the FPGA need to make with the analog board is done through this connector so the only other signals coming onto the board are the hydrophones and power.

IV. SOFTWARE

VHDL was the language of choice for use on the Xilinx Spartan 3e due to some of the available libraries for serial communication and interface to the Digilent PmodAD1. The following are descriptions of the various components that was utilized within the FPGA to complete the assigned tasks of APL subsystem.

Analog Sample Component is responsible for interfacing with the three individual PmodAD1 configured on the analog board. It ensures simultaneous analog to digital conversions by all five analog input channels and outputs a synchronization signal for every valid sample captured.

PmodAD1 Reference Component contains all the code to properly interface with the Digilent PmodAD1 hardware high speed analog to digital converter. Communication to the device is done over the standard SPI protocol, the

higher logic is insulated from low level bit shifting by utilizing this component provided by Digilent Incorporated [1].

Channel Component is a high level component that contains no processes it simply wires the sub components that are required for each individual channel. It was abstracted this way to provide for ease of expandability for multiple channels. This component contains the DC Calculate Component, the Peak to Peak Component, Ping Detect Component, and Adder Component.

DC Calculate Component is a sub component of the Channel Component that calculates the DC value of the received analog signal by implementing a digital low pass filter on the values. The calculated DC value is utilized by the Adder Component to properly control the digital pot that enable the level shifting that centers the signal from 0V to 1.65V due to the fact that the PmodAD1 analog to digital converter does not support negative voltage only from the range of 0.0V to 3.3V.

Peak to Peak Component is a sub component of the Channel Component and stores the max and min values of the received signals that are utilized for controlling the gain of the Variable Gain Amplifiers of the pre and post amp of each channel controlled through the Arbiter Component. This ensures that the operation amplifiers never saturate and the heavily attenuated signals can be properly gained for capturing and analysis.

Ping Detect Component is a sub component of the Channel Component that determines when a proper ping has occurred. For the proper analysis to be performed on the signals it has to be ensured that the signal is not echoes of the pinger or a random noise spike from the environment. This component utilizes the DC Calculated value to determine the “silence” value of the signal the time when the pinger is off. The length of time for “silence” is calculated and has to exceed some tested value. After the silence time is exceeded the component is then listening for the leading edge of the ping that has to exceed some threshold value from the DC Calculated Value. Once all conditions have been met the component sets an output flag for the rest of the system of ping detected.

Adder Component is a sub component of the Channel Component that performs the control logic for the level shift of the analog signal just before being captured by the ADC. This component utilizes the DC calculated value of the signal to determine the offset value from the desired center of 1.65V and the system is updated about twice a second to allow for all values to stabilize once updated.

Sample Frequency Component takes input from the Analog Sample Component to calculate both the sample frequency and period for the conversions that can be

utilized later for the performing the mathematical analysis on the signals. The measurements are all based on the base clock frequency on the FPGA of 50 MHz.

Arbiter Component takes is responsible for controlling the analog hardware channels and fuses the values of all channels to ensure that the channels gains are equivalent as to not introduce unintended phase shifts at various stages unequal to each channel. Based on the method of analysis this is necessary for maintaining accuracy.

Digital Potentiometer Controller Component contains several sub components that control the DS1803 digital potentiometer chips utilizing the DS1803 Interface Component. This component is designed to update all the DS1803 chips at a specified time interval. All digital potentiometers are updated asynchronously due to the use of the I2C interface allowing only single serial messages.

DS1803 Interface Component is a sub component of the Digital Potentiometer Controller and contains all the custom logic to send commands to the DS1803 chips utilizing I2C provided by the I2C Component.

I2C Component provides a simple interface to utilizing the Philips I2C bus standard from a library hosted on OpenCores [2].

MAX268 Filter Interface Component provides a high level interface to setting the MAX268 Filter chip. This component contains a sub component necessary for configuring the MAX268 Filter the Square Wave Component. All the available frequencies were pre-computed and stored in the FPGA by a look up table. This encapsulates the user from having to know all the specifics of the MAX268 Filter provided in the datasheet to simply selecting a frequency.

Square Wave Component was a custom component that generates a constant 50% duty cycle pulse width modulated signal or square wave at varying frequencies and is utilized in the MAX268 Filter Component.

MCU Packet Receiver Transmitter Component is responsible for the communication of valid MCU packets between the FPGA and the host computer. This component is compliant with the packet format specified in the MCU Library of the Robotics Club at UCF Zebulon repository. The communication protocol is over the RS232 Standard and utilizes the RS232 Reference Component for sending and receiving individual bytes.

RS232 Reference Component is a simple interface to utilize the RS232 Standard for communicating serial data provided by Digilent Incorporated [3].

V. MATHEMATICAL ANALYSIS

After conducting research in the subject matter of acoustic localization, currently there are several known

techniques for obtaining the unknown position of the emitter with a set of receivers. The following sections will describe the analysis of each technique and conclude with the features and drawbacks of the particular method.

The following is an overall description of the problem with known and unknown information obtained by the system: The acoustic pinger is located underwater at some unknown position with a specified ping duration, period, and approximate frequency. The Acoustic Pinger Locator passively listens for the acoustic ping produced by the pinger and captures the sound waves via an underwater microphone, known as a hydrophone, converting the sound energy into an electrical signal of voltage versus time. The voltage of the electrical signal generated is proportional to the strength of the sound wave. Once the sound waves produced by the underwater acoustic pinger are captured, analysis and processing needs to be performed on the received signals to calculate the location of the ping source.

A. Multilateration

Multilateration, also known as hyperbolic positioning and is utilized for localizing the emitter. This process utilizes the computation of the time difference of arrival of the signal to the set of receivers. Multilateration measures the time differences between the receivers and through the math generates three-dimensional hyperboloid meshes where the intersection is the location of the emitter. The mathematical analysis is nonlinear and certain issues arose through an initial simulation and testing of the system.

Our senior design team designed a sophisticated and thorough computer simulation. With the use of the simulator the closed form solution of the multilateration method was confirmed. Further testing was performed to test the accuracy and precision of the algorithm by using a technique known as brute force method. Pinger positions were iterated through a 10 meter by 10 meter by 10 meter volume and error measurements were taken. The results proved to be successful.

An additional step was followed to determine the precision and accuracy of the algorithm given some error through the input of the system. It was discovered that with only a 1% error of difference in the timing on one of the input signals the output diverged significantly from the desired solution. This correlates to the non-linearity of the system and proves to be unstable and cannot be utilized in the application of the acoustic pinger locator as less than 1% error cannot be ensured.

B. Data Mapping

With the system being non-ideal and prone to error, a more robust method for calculating the heading and distance to the pinger is desired. Further research was conducted and data mapping was discovered. Data mapping is the process of creating data element mappings between two separate and distinct sets, the input of hydrophone timing information and the output of the heading and distance to the pinger. With the system inherently being non-linear as described in the multilateration section, this poses to be a difficult problem. Data mapping is a technique that attempts to linearize the system about some non-linear function and reduce the error to within some specified tolerance. This technique is currently being tested and will eventually be completely implemented on the APL subsystem.

VI. TIMING ACQUISITION TECHNIQUES

Acquiring synchronized and accurate timing of the emitter's signal to each individual hydrophone of the array requires specialized hardware and techniques. Through our research we discovered several different methods for solving this problem. Each of the methods has different strengths and weaknesses based on complexity, accuracy, being prone to error, and adaptability.

A. Counter Method

One of the more simple methods is implemented using high speed counter to measure the time differences for each hydrophone; this will be referred to as the counter method. This method utilizes the analog output from each of the hydrophones that is then compared to some reference voltage that triggers a high speed timer. Addition logic is required for the full implementation. One high speed timer would be utilized for the set of the hydrophones, the trigger for the high speed timer would be or'ed with all the comparators with the hydrophones. The output of each comparators would also set a latch and set a register of the current timer value. After all latches are set the timing capture would be captured and the registers that hold the timer values for each hydrophone would be read into some processor to implement one of the acoustic locating techniques.

B. Frequency Domain Analysis (Phase Shifts)

Analyzing in the frequency domain gives constraints to the system, such as maintaining the distance within each hydrophone to be one half wavelength of the signal. The transformation of the data from the time domain in which the signals are captured to the frequency domain in how the signals will be analyzed is through the Fourier

Transform, more specifically for our system, the discrete fast Fourier transform. To analyze in the frequency domain with digital hardware the signals need to be captured from its form of an analog signal of continuous voltage and continuous time a digital form of discrete values of voltage to discrete time. For sampling the data, the Nyquist Sampling theorem needs to be satisfied, that is the sampling period needs to be at least twice of the highest frequency component of the signal to prevent anti-aliasing of the captured signal. This requires that the system needs analog filters to attenuate all high frequencies and high speed analog to digital converters that samples at least twice the speed of the pinger frequency.

C. Cross Correlation(Signal Time Shifts)

In signal processing, the process of measuring the similarity between two waveforms as a function of a time-shift applied to one of the waveforms is known as cross correlation. Imagine taking the two hydrophone signals that are separated an arbitrary distance away. If the signal from the pinger is propagating through the water at certain wave-speed one of the hydrophones will start to receive the signal first and the other at a later point in time however, the wave-shape should be exactly the same. The only difference between the two would be attenuation of amplitude for the second hydrophone relative to the first hydrophone. Cross correlation is a good fit for this type of signal analysis as the two signals are only different by a shift in time.

Utilizing cross correlation for deriving the timing for the set of hydrophone signals is a robust method as it is not dependent on the signal being a pure sine wave, it can take any arbitrary shape, and the hydrophone array does not need to be configured in such a limiting manner of one-half wavelength as in the frequency domain analysis method. Cross correlation does have its limitations though, with the discretized signals the highest resolution is based on the actual sample frequency of system therefore, the higher the sampling rate the more distinct values of time shifting can be achieved. Also, provided the system has enough memory to capture the amount of data for the extreme case, the hydrophones can be spread out further for higher resolution.

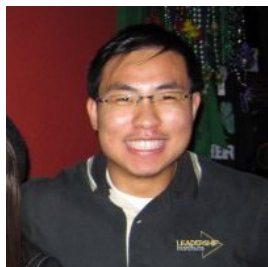
VII. CONCLUSION

The preliminary design consists of an array of four or five hydrophones arranged in a particular way to allow for phase analysis on the signals to triangulate a heading, depth, and distance. Several different techniques were researched to achieve acoustic localization, a simulator was created to perform some preliminary analysis on these

different methods to facilitate a final design. Another important aspect of this project is to receive the acoustic pinger signals from the underwater environment. The proposed method of achieving this goal is a passive hydrophone array mounted on the vehicle that converts acoustic energy into electrical energy. These attenuated signals are then conditioned by first pre-amplification with a variable gain to a utilizable signal. The signal is then filtered at the pinger's specified frequency using a fourth order Butterworth bandpass filter to remove unwanted noise. The final analog signal processing stage needs to adjust the signal for the appropriate range of the analog to digital converter.

The analog signals are captured simultaneously from the analog to digital converter at a sampling rate that exceeds the Nyquist sampling theorem to receive unaliased digital signal data. The data is then processed by an FPGA which contains the digital signal processing to calculate the acoustic localization of the pinger. The first step is to analyze each individual hydrophone signal by performing the FFT on the signals and determine relative phase differences between the hydrophone signals. The phase differential information is then used in the mathematical multilateration technique implemented on the FPGA to calculate the pingers location. The pingers heading, depth, and distance relative to the hydrophone array is then communicated over serial to the AUV's host computer which is then used to navigate to the pinger in the competition.

THE ENGINEERS



Zhen Cai is a senior student of the Computer Engineering department at University of Central Florida. He is currently interning at Lockheed Martin Missiles and Fire Control facility. He will continue his master degree at University of Central Florida in the Fall of 2011.



Jonathan Mohlenhoff is 23 years old and is graduating with a Bachelor of Science in Electrical Engineering within the College of Engineering and Computer Science at the University of Central Florida. He is enrolled for the fall semester of 2010 for continuing

his education with Masters in Electrical Engineering concentrating in electromagnets and signal processing. He has received a full scholarship for graduate school from the DoD through the SMART Scholarship Program and will be interning with the Air Force at Robin's AFB, Georgia. He has had a Professional Internship with the Walt Disney World Co. in Sustaining Engineering and currently works as an Undergraduate Research Assistant in the ACTIVE Lab at the Institute for Simulation and Training (IST) of UCF. He has also been very involved in extracurricular activities through the Robotics Club at UCF as the current President and has previously been team leader for several of the projects.



Cassandra Puklavage will be graduating with a Bachelor of Science in Electrical Engineering within the College of Engineering and Computer Science at the University of Central Florida. She received the Provost Fellowship from UCF and will be pursuing a Masters in Computer Engineering in the fall semester of 2010. She will follow the ISML (Intelligent Systems and Machine Learning) track. She is currently working as an undergraduate researcher in the ISL (Intelligent Systems Lab) of UCF. She is also very involved with the Robotics Club at UCF both as a serving officer and the current team leader of the AUV (Autonomous Underwater Vehicle) project.

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REFERENCES

- [1] Digilent Incorporated [Internet]. Pullman (WA): PmodAD1 Reference Component; c2006-2010 [modified 2009 April 20; cited 2010 April 10]. Available from: <http://www.digilentinc.com/Data/Products/PMOD-AD1/PmodAD1%20RefComp.zip>.
- [2] OpenCores [Internet]. Sweden (Europe): I2C Controller Core; c1999-2010 [modified 2010 March 5; cited 2010 April 10]. Available from: <http://www.opencores.org/project,i2c>.
- [3] Digilent Incorporated [Internet]. Pullman (WA): RS232 Interface Reference Component; c2006-2010 [modified 2009 April 20; cited 2010 April 10]. Available from: <http://www.digilentinc.com/Data/Documents/Reference%20Designs/RS232%20RefComp.zip>.